What is claimed is:

1. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a material layer having a plurality of vaporization temperatures, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

2. The integrated circuit assembly of claim 1, wherein the electronic chip is a memory chip.

3. The integrated circuit assembly of claim 2, wherein the memory chip is a dynamic random access memory chip.

4. The integrated circuit assembly of claim 1, wherein the conductive structure is fabricated from copper.

5. The integrated circuit assembly of claim 1, wherein at least one of the plurality of vaporization temperatures is about 400 degrees centigrade.

6. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a plurality of materials, each of the plurality of materials having a different vaporization temperature, the plurality of materials is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

7. The integrated circuit assembly of claim 6, wherein the electronic chip is an analog signal processing chip.

8. The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is silicon dioxide.

9. The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is carbon.

10. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a material layer having a structural component having a structural vaporization temperature and a non-structural component having a non-structural vaporization temperature less than the structural vaporization temperature, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

11. The integrated circuit assembly of claim 10, wherein the electronic chip is a digital signal processor.

12. The integrated circuit assembly of claim 10, wherein the structural component is fabricated from silicon dioxide.

13. The integrated circuit assembly of claim 12, wherein the silicon dioxide is a low temperature silicon dioxide.

14. The integrated circuit assembly of claim 10, wherein the non-structural component is fabricated from carbon.

15. The integrated circuit assembly of claim 10, wherein the non-structural component is fabricated from a polymer.

16. The integrated circuit assembly of claim 15, wherein the polymer is a photoresist.

17. The integrated circuit assembly of claim 10, wherein the electronic chip is comprised of logic circuits.

18. An integrated circuit assembly comprising:

an electronic chip;

a support structure mounted on the electronic chip, the support structure having an interstice and a vaporization temperature;

a material filling the interstice, the material having a vaporization temperature that is less than the vaporization temperature of the support structure;

a connective structure mounted on the support structure; and

a conductive structure capable of coupling the electronic chip to the connective structure, the conductive structure embedded in the support structure and the material.

19. The integrated circuit assembly of claim 18, wherein the electronic chip is a dynamic random access memory chip.

20. The integrated circuit assembly of claim 18, wherein the support structure is fabricated from silicon dioxide.

21. The integrated circuit assembly of claim 18, wherein the support structure is a ribbed structure.

22. The integrated circuit assembly of claim 18, wherein the material is carbon dioxide.

23. The integrated circuit assembly of claim 18, wherein the connective structure is a controlled collapse chip connection (C4) structure.

24. The integrated circuit assembly of claim 18, wherein the conductive structure is fabricated from a copper alloy.

25. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure including a support structure, the conductive structure having a vaporization temperature and the conductive structure including the support structure is embedded in a material layer having a vaporization temperature less than the vaporization temperature of the conductive structure, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

26. The integrated circuit assembly of claim 25, wherein the electronic chip is a microprocessor.

27. An integrated circuit memory device comprising:

an electronic memory chip; and

a ribbed structure mounted on the electronic memory chip and capable of protecting an air-bridge structure and supporting a C4 structure.

28. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from an inorganic insulator.

29. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from an organic material.

30. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from of a mix of organic and inorganic materials.

31. An integrated circuit assembly comprising:

an electronic chip; and

a post structure mounted on the electronic chip and capable of protecting an air-bridge structure and supporting a C4 structure.

32. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from the same material as the air-bridge structure.

33. The integrated circuit assembly of claim 31, wherein the post structure is mounted on an insulating base formed on the electronic chip.

34. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from an insulator.

35. The integrated circuit assembly of claim 31, wherein the insulator is silicon dioxide.

36. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from a polymer.

37. The integrated circuit assembly of claim 36, wherein the polymer is polyimide.

38. An integrated circuit assembly comprising:

an electronic chip including a plurality of electronic devices;

a plurality of conductive segments capable of interconnecting the plurality of electronic devices, each of the plurality of conductive segments having a surface area in contact with a material having a dielectric constant of about 1;

a C4 connection coupled to the electronic chip through the plurality of conductive segments; and

a substrate coupled to the C4 connection.

39. The integrated circuit assembly of claim 38, wherein the integrated circuit assembly is hermetically sealed.

40. The integrated circuit assembly of claim 39, wherein the integrated circuit assembly is back filled with helium.

41. The integrated circuit assembly of claim 39, wherein the integrated circuit assembly is back filled with a helium rich gas mixture.

42. The integrated circuit assembly of claim 38, wherein the material is air.

43. The integrated circuit assembly of claim 38, wherein the material is a foam.

44. The integrated circuit assembly of claim 38, further comprising a heat sink coupled to the electronic chip.

45. The integrated circuit assembly of claim 44, wherein the integrated circuit assembly is hermetically sealed.`

46. The integrated circuit assembly of claim 45, wherein the integrated circuit assembly is back filled with helium.

47. A computer system comprising:

a processor;

a memory device having a plurality of circuit devices, the memory device coupled to the processor; and

an air-bridge structure and a support structure fabricated on the memory device, the air-bridge structure capable of coupling at least two of the plurality of circuit devices and the support structure capable of supporting the memory device mounted as a flip chip.

48. The computer system of claim 47, wherein the air-bridge structure is embedded in a dielectric having a dielectric constant of about 1.

49. The computer system of claim 47, wherein the support structure fabricated on the memory device is a ribbed support structure.

50. A method of constructing an integrated circuit comprising:

fabricating a plurality of electronic devices on a substrate;

embedding a wiring structure in a plurality of materials having a plurality of vaporization temperatures, the plurality of materials is located on the substrate and the wiring structure interconnects the plurality of electronic devices;

mounting the integrated circuit on a packaging substrate; and

removing at least one of the plurality of materials after the integrated circuit is mounted on the packaging substrate.

51. The method of claim 50, further comprising:

attaching a C4 structure to the integrated circuit prior to mounting the integrated circuit on the packaging substrate.

52. The method of claim 51, wherein removing at least one of the plurality of materials after the integrated circuit is mounted on the packaging substrate comprises:

heating the integrated circuit.

53. The method of claim 52, wherein heating the integrated circuit comprises:

placing the integrated circuit in a furnace having an oxygen atmosphere heated to about 400 degrees centigrade.

54. A method of forming an air bridge structure comprising:

forming a support structure having a support structure vaporization temperature and having interstices on an electronic chip;

filling the interstices of the support structure with a fill material having a vaporization temperature that is less than the support structure vaporization temperature;

embedding a conductive structure in the support structure and the material;

mounting a connective structure on the support structure; and

removing the fill material.

55. The method of claim 54, wherein forming a support structure having a support structure vaporization temperature and having interstices on an electronic chip comprises:

depositing a layer of silicon dioxide on the electronic chip; and

etching the layer of silicon dioxide to form the support structure having interstices.

56. A method of forming an air bridge structure comprising:

forming a support structure having interstices on an electronic chip;

filling the interstices of the support structure with a fill material having a vaporization temperature that is less than the vaporization temperature of the support structure;

embedding a conductive structure in the fill material;

mounting a connective structure on the support structure; and

vaporizing the fill material.

57. The method of claim 56, wherein filling the interstices of the support structure with a material having a vaporization temperature that is less than the vaporization temperature of the support structure comprises:

depositing a layer of carbon on the electronic chip.

58. The method of claim 57, wherein depositing a layer of carbon on the electronic chip comprises:

sputtering the layer of carbon on the electronic chip.

59. The method of claim 58, further comprising:

planarizing the layer of carbon.

60. A method of forming an air bridge structure comprising:

forming a material layer on an electronic chip;

embedding a conductive structure and a conductive support structure in the material layer, the conductive structure is capable of electronically coupling to the electronic chip; and

removing the material layer.

61. The method of claim 60, wherein embedding a conductive structure and a conductive support structure in the material layer comprises:

etching the material layer to form a plurality of vertical wiring vias and a plurality of vertical support vias;

etching a wiring pattern in the material layer; and

applying a conductive material to the plurality of vertical wiring vias, the plurality of vertical support vias, and the wiring pattern.

62. The method of claim 61, wherein removing the material comprises:

vaporizing the material.

63. The method of claim 62, wherein vaporizing the material comprises:

processing the integrated circuit assembly in a furnace having an oxygen atmosphere at a temperature of approximately 400 degrees centigrade.

64. A method of forming an air bridge structure comprising:

forming a material layer on an electronic chip;

embedding a conductive structure and a conductive support structure in the material layer, the conductive structure is capable of being electronically coupled to the electronic chip;

mounting a connective structure on the support structure; and

removing the layer material.

65. The method of claim 64, further comprising:

attaching a heat sink to the electronic chip.

66. A method of packaging an integrated circuit comprising:

fabricating an integrated circuit structure including a conductive structure and a ribbed support structure embedded in a fill material;

mounting C4 pads on the integrated circuit structure;

mounting the integrated circuit structure on a substrate;

removing the fill material; and

backfilling with a gas and hermetically sealing the substrate.

67. The method of claim 66, wherein the gas is helium.

68. The method of claim 66, wherein the fill material is carbon.

69. The method of claim 66, wherein the fill material is a high temperature polymer.

70. The method of claim 66, wherein the high temperature polymer is polyimide.

71. The method of claim 66, where the structural material is a metal.

72. The method of claim 71, wherein the metal is copper.

73. The method of claim 66, wherein the structural material is SiO_2.

74. The method of claim 66, wherein the structural material is Si_3N_4.